



US007293155B2

(12) **United States Patent**  
**Mehta et al.**

(10) **Patent No.:** **US 7,293,155 B2**

(45) **Date of Patent:** **Nov. 6, 2007**

(54) **MANAGEMENT OF ACCESS TO DATA FROM MEMORY**

(75) Inventors: **Kalpesh Dhanvantrai Mehta**, Chandler, AZ (US); **Wen-Shan Wang**, Chandler, AZ (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

6,279,096	B1 *	8/2001	McCoy et al. ....	711/211
6,397,324	B1 *	5/2002	Barry et al. ....	712/225
6,453,367	B2 *	9/2002	Barry .....	710/26
6,453,402	B1 *	9/2002	Jeddeloh .....	711/167
6,457,073	B2 *	9/2002	Barry et al. ....	710/22
6,463,518	B1 *	10/2002	Duboc .....	711/220
6,581,152	B2 *	6/2003	Barry et al. ....	712/24
2002/0004916	A1 *	1/2002	Marchand et al. ....	713/322
2004/0153524	A1 *	8/2004	Kang et al. ....	709/213

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 365 days.

(21) Appl. No.: **10/449,316**

(22) Filed: **May 30, 2003**

(65) **Prior Publication Data**

US 2004/0250042 A1 Dec. 9, 2004

(51) **Int. Cl.**  
**G06F 12/00** (2006.01)

(52) **U.S. Cl.** ..... **711/206; 711/214; 711/217; 711/218**

(58) **Field of Classification Search** ..... **711/206, 711/214, 217, 218, 221**  
See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

3,634,828	A *	1/1972	Myers et al. ....	358/1.3
4,935,867	A *	6/1990	Wang et al. ....	711/217
5,206,940	A *	4/1993	Murakami et al. ....	711/218
6,021,473	A *	2/2000	Davis et al. ....	711/141
6,180,864	B1 *	1/2001	Furuhashi et al. ....	84/603
6,260,082	B1 *	7/2001	Barry et al. ....	710/22

**OTHER PUBLICATIONS**

Jean-Loup Baer, "Computer System Architecture," Computer Science Press, 1980, pp. 379-380.\*

\* cited by examiner

*Primary Examiner*—Matthew Kim

*Assistant Examiner*—Sheng-Jen Tsai

(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

Arbitrary patterns of address locations of digital data can be efficiently read from a memory of a signal processor. For example, a first memory address generator receives a first memory command signal from a first communication register to retrieve a first set of data from memory according to a look up table of memory addresses. The first memory access generator reads the look up table of memory addresses, which contain a second set of memory commands and reroutes the second set of commands to a bypass register. In turn, the second set of memory commands stored at the bypass register are read by a second memory address generator which retrieves a second set of data from memory according to the second set of memory command signals read out of memory by the first memory address generator.

**28 Claims, 10 Drawing Sheets**

