



US007152167B2

(12) **United States Patent**  
**Kurts et al.**

(10) **Patent No.:** **US 7,152,167 B2**  
(45) **Date of Patent:** **Dec. 19, 2006**

- (54) **APPARATUS AND METHOD FOR DATA BUS POWER CONTROL** 6,141,765 A \* 10/2000 Sherman ..... 713/400  
6,330,679 B1 12/2001 Conary et al.
- (75) Inventors: **Tsvika Kurts**, Haifa (IL); **Doron Orenstien**, Haifa (IL); **Marcelo Yuffe**, Binyamina (IL) 6,339,552 B1 \* 1/2002 Taruishi et al. .... 365/189.05  
6,643,792 B1 \* 11/2003 Kurosawa ..... 713/501
- (73) Assignee: **Intel Corporation**, Santa Clara, CA (US) 2001/0037421 A1 11/2001 Singh et al.  
2003/0126485 A1 7/2003 Wilcox et al.  
2003/0131125 A1 7/2003 Ooi  
2004/0117670 A1 6/2004 Kurts et al.

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 357 days.

**FOREIGN PATENT DOCUMENTS**

- (21) Appl. No.: **10/317,776** EP 0 932 097 A1 7/1999  
WO WO 03/058467 A1 7/2003
- (22) Filed: **Dec. 11, 2002**

**Prior Publication Data**

(65) US 2004/0117670 A1 Jun. 17, 2004

(51) **Int. Cl.**  
**G06F 1/26** (2006.01)  
**G11C 5/14** (2006.01)

(52) **U.S. Cl.** ..... **713/300**; 713/323; 365/227

(58) **Field of Classification Search** ..... 713/300,  
713/310, 323, 400; 365/207, 194, 189, 227;  
710/301

See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

- 4,862,348 A 8/1989 Nakamura
- 4,947,379 A \* 8/1990 Okuyama ..... 365/233.5
- 5,327,394 A \* 7/1994 Green et al. .... 365/233.5
- 5,432,944 A 7/1995 Nuckolls et al.
- 5,737,746 A \* 4/1998 Hardin et al. .... 711/118
- 5,819,027 A \* 10/1998 Budelman et al. .... 714/47
- 5,848,428 A 12/1998 Collins
- 5,884,088 A 3/1999 Kardach et al.
- 5,915,121 A 6/1999 Wagner
- 6,058,059 A \* 5/2000 Huang et al. .... 365/207
- 6,073,195 A \* 6/2000 Okada ..... 710/301
- 6,076,140 A 6/2000 Dhong et al.

**OTHER PUBLICATIONS**

Snyder, Jeffrey, "New Pentium M Brings Integrated Graphics, I/O to Low-Power Embedded Apps", COTS Journal, May 2004, <http://www.cotsjournalonline.com/home/printthis..php?id=100119>, <http://www.cotsjournalonline.com/home/article..php?id=100119>.

(Continued)

*Primary Examiner*—Thomas Lee  
*Assistant Examiner*—Suresh K Suryawanshi  
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

An approach for data bus power control. Data input sense amplifiers of a request agent are enabled prior to a data phase of a transaction according to a data bus power control signal. Once enabled, the data input sense amplifiers can capture data provided during the data phase of the read transaction. Accordingly, the data input sense amplifiers of the request agent are disabled according to the power control signal once the data phase of the read transaction is complete.

**55 Claims, 14 Drawing Sheets**

