



US005914711A

United States Patent [19] Mangerson et al.

[11] Patent Number: **5,914,711**
[45] Date of Patent: **Jun. 22, 1999**

[54] **METHOD AND APPARATUS FOR BUFFERING FULL-MOTION VIDEO FOR DISPLAY ON A VIDEO MONITOR**

[75] Inventors: **Mark M. Mangerson**, LeMars, Iowa;
Randall S. Farwell, Dakota Dunes, S. Dak.

[73] Assignee: **Gateway 2000, Inc.**, North Sioux City, S. Dak.

[21] Appl. No.: **08/638,769**

[22] Filed: **Apr. 29, 1996**

[51] Int. Cl.⁶ **H04N 7/12**

[52] U.S. Cl. **345/203; 345/507; 345/508**

[58] Field of Search **345/185, 189, 345/201, 507, 508, 203; 348/441, 448, 422; 395/118, 501, 507-509, 512**

[56] References Cited

U.S. PATENT DOCUMENTS

4,698,674	10/1987	Bloom	358/140
4,719,509	1/1988	Sakamoto	358/112
4,814,873	3/1989	Maekawa	358/140
4,855,813	8/1989	Russell et al.	358/22
4,862,269	8/1989	Sonoda et al.	358/160
4,994,912	2/1991	Lumelsky et al.	358/140
5,053,864	10/1991	Thompson	358/22
5,249,164	9/1993	Koz	358/21 R
5,274,753	12/1993	Roskowski et al.	395/135
5,291,275	3/1994	Lamelsky	348/441
5,347,322	9/1994	Levine et al.	348/718

5,402,147	3/1995	Chen et al.	345/115
5,461,679	10/1995	Normile et al.	382/304
5,473,383	12/1995	Sezan et al.	348/452
5,519,449	5/1996	Yanai et al.	348/598
5,534,936	7/1996	Kim	348/448
5,557,302	9/1996	Levinthal et al.	345/189
5,557,332	9/1996	Koyanagi et al.	398/416
5,594,467	1/1997	Marlton et al.	345/115
5,633,687	5/1997	Bhayani et al.	348/441
5,668,599	9/1997	Cheney et al.	348/409

Primary Examiner—Jeffery Brier
Assistant Examiner—Vincent E. Kovalick
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.; Anthony Claiborne

[57] ABSTRACT

Triple-buffering video memory in a computer graphics controller improves the quality of full-motion video converted for display on a computer monitor. Buffer size, organization, and access cycles prevent converted data representing a new video frame from overwriting a buffer in memory that contains converted data representing a video frame currently being displayed. The access cycles also ensure all data representing a video frame is displayed. The video memory is partitioned into three logical buffers to hold the converted data, the buffers are arranged in a logical ring sequence for read and write access, and the data in a buffer is repeatedly read until the next buffer in the sequence is full of data and ready to be read. In addition, the buffering is adaptable to different resolutions as the size of the buffers is determined by the value of the resolution each time the video conversion is initiated.

13 Claims, 6 Drawing Sheets

