US005892377A

United States Patent [19]

Johnston et al.

[11] **Patent Number: 5,892,377**

[45] **Date of Patent: Apr. 6, 1999**

[54] **METHOD AND APPARATUS FOR REDUCING LEAKAGE CURRENTS IN AN I/O BUFFER**

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[21] Appl. No.: **621,395**

[22] Filed: **Mar. 25, 1996**

[51] **Int. Cl.**[6] **H03K 3/00**

[52] **U.S. Cl.** **327/108**; 327/170; 327/377; 327/437; 327/540; 326/83; 326/86

[58] **Field of Search** 327/108–112, 374–377, 327/170, 379, 389, 391, 427, 434, 437, 540, 382, 383, 387, 309, 310, 312, 314, 318–324, 331, 332; 326/21, 27, 81, 83

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[57] **ABSTRACT**

A method and apparatus for reducing leakage currents in a high voltage tolerant I/O buffer. An I/O buffer designed to tolerate high external voltages by blocking such voltages at a passgate in a p-output path that uses a device between a p-driver gate node and a p-gate node of the passgate to ensure that the p-transistor of the passgate is turned on when the p-driver is driving the pad high. A second device isolates the p-gate node of the passgate from the pad until a pad voltage reaches a predetermined level. Once the pad voltage reaches the predetermined level, the device drives the voltage at the p-gate node of the passgate to that of the pad. Maintaining the p-transistor of the passgate on while the p-driver is driving the pad high allows a rapid hard shut-off of the p-driver as the I/O buffer tri-states the pad. Additionally, the second device maintains the necessary voltage protection by insuring a hard shut-off of the p-transistor of the passgate when the voltage at the pad reaches a predetermined level.

14 Claims, 3 Drawing Sheets